Docket No.: P2001,0325

MAIL STOP: APPEAL BRIEF-PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

Applic. No.	:	10/701,058	Confirmation No.: 5559
Inventor	:	Holger Sedlak, et al.	
Filed	:	November 4, 2003	
Title	:	Frequency Regulating Circuit	
TC/A.U.	:	2836	
Examiner	:	Dru M. Parries	
Customer No.	:	24131	

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in **the final Office Action** dated May 11, 2007, finally rejecting claims 1, 3, 4, 6, 7 and 9.

Appellants submit this *Brief on Appeal* including payment in the amount of $500.00 to cover the fee for filing the *Brief on Appeal*.

<u>Real Party in Interest</u>:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

<u>Related Appeals and Interferences</u>:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

<u>Status of Claims</u>:

Claims 1, 3, 4, 6, 7 and 9 are rejected and are under appeal. Claims 2, 5 and 8 were cancelled in an amendment filed May 31, 2006.

<u>Status of Amendments</u>:

No claims were amended after the final Office action. *A response under 37 CFR § 1.116* was filed on July 11, 2007. The Primary Examiner stated in an *Advisory Action* dated August 6, 2007 that the request for reconsideration had been considered but did not place the application in condition for allowance.

<u>Summary of the Claimed Subject Matter</u>:

The invention relates to a frequency regulating circuit for circuit configurations.

Independent claim 1:

A frequency regulating circuit [Fig. 1; page 6, lines 14 - 15] for the current-consumption-dependent clock supply of a circuit configuration [1 of Fig. 1] [page 3, lines 1 - 3], comprising:

a current measuring device [2 of Fig. 1; page 6, line 26 - page 7, line 1] for measuring an instantaneous current consumption of the circuit configuration [1 of Fig. 1] [page 4, line 25 - page 5, line 2];

means for comparing [12 of Fig. 1] the instantaneous current measured by said current measuring device [2 of Fig. 1] with a definable threshold value [13 of Fig. 1] [page 8, lines 7 - 10];

a controllable clock supply circuit [4 of Figs. 1 and 2] having:

> an output [6 of Figs. 1 and 2] to be connected to a clock input [11 of Fig. 1] of the circuit configuration [1 of Fig. 1] [page 7, lines 5 - 7];
>
> a clock generator [7 of Fig. 2] generating a clock signal with clock pulses [See Fig. 2], said clock generator [7 of Fig. 2] generating a constant maximum internal frequency [See Fig. 2] [page 7, lines 24 - 26]; and
>
> a pulse filter [8 of Fig. 2] for filtering clock pulses from said clock signal from said clock generator [7 of Fig. 2], said pulse filter [8 of Fig. 2] including a

control input [5 of Fig. 2], a filtered clock signal being provided to said output [See Fig. 2] [page 7, line 26 - page 8, line 5];

a control device [3 of Fig. 1] connected to said clock supply circuit [4 of Figs. 1 and 2] and driving said clock supply circuit [4 of Figs. 1 and 2] based upon the measured current consumption [page 7, lines 1 - 15], said control device [3 of Fig. 1] providing a control signal to said control input [5 of Figs. 1 and 2] of said pulse filter [8 of Fig. 2] when said means for comparing [12 of Fig. 1] determine that the instantaneous current consumption exceeds the definable threshold value [from 13 of Fig. 1] [page 7, lines 9 - 15]; and

said pulse filter [8 of Fig. 2] suppressing an individual clock pulse of said clock signal [page 7, line 26 - page 8, line 5] generated by said clock signal generator [4 of Figs. 1 and 2], in response to said control signal at said control input [5 of Figs. 1 and 2], such that said control device [3 of Fig. 1] adjusts said clock frequency to provide at said output [6 of Figs. 1 and 2], at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit [1 of Fig. 1] [page 5, lines 2 - 5; page 7, lines 9 - 21].

Independent claim 4:

4. A frequency regulating circuit [Fig. 1; page 6, lines 14 - 15] for the current-consumption-dependent clock supply of a circuit configuration [1 of Fig. 1] [page 3, lines 1 - 3], comprising:

a current measuring device [2 of Fig. 1; page 6, line 26 - page 7, line 1] for measuring an instantaneous current consumption of the circuit configuration [page 4, line 25 - page 5, line 2];

means for comparing [12 of Fig. 1] the instantaneous current measured by said current measuring device [2 of Fig. 1] with a definable threshold value [13 of Fig. 1] [page 8, lines 7 - 10];

a controllable clock supply circuit [4 of Figs. 1 and 2] having:

an output [6 of Figs. 1 and 2] to be connected to a clock input [11 of Fig. 1] of the circuit configuration [1 of Fig. 1] [page 7, lines 5 - 7];

a clock generator [7 of Fig. 2] generating a clock signal with clock pulses, said clock generator [7 of Fig. 2] generating a constant maximum internal frequency [See Fig. 2] [page 7, lines 24 - 26]; and

a pulse filter [8 of Fig. 2] connected to at least one of said clock generator [7 of Fig. 2] and said output [6 of Figs. 1 and 2], for filtering clock pulses from said clock signal from said clock generator [7 of Fig. 2], said pulse filter [8 of Fig. 2] including a control input [5 of Figs. 1 and 2], a filtered clock signal being provided to said output [6 of Figs. 1 and 2] [page 7, line 26 - page 8, line 5];

a control device [3 of Fig. 1] connected to said clock supply circuit [4 of Figs. 1 and 2] and driving said clock supply circuit [4 of Figs. 1 and 2] based upon the measured current consumption [page 7, lines 1 - 15], said control device [3 of Fig. 1] programmed to provide a control signal to said control input [5 of Figs. 1 and 2] of said pulse filter [8 of Fig. 2] when said means for comparing [12 of Fig. 1] determines that the instantaneous current consumption exceeds the definable threshold value [from 13 of Fig. 1] [page 7, lines 9 - 15]; and

said pulse filter [8 of Fig. 2] suppressing an individual clock pulse of said clock signal [page 7, line 26 - page 8, line 5] generated by said clock signal generator [7 of Fig. 2], in response to said control signal at said control input [5 of Figs. 1 and 2], such that, said control device [3 of Fig. 1] adjusts said clock frequency to provide at said output [6 of Figs. 1 and 2], at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit [page 5, lines 2 - 5; page 7, lines 9 - 21].

Independent claim 7:

A frequency regulating circuit [Fig. 1; page 6, lines 14 - 15] for the current-consumption-dependent clock supply of a circuit configuration [1 of Fig. 1] [page 3, lines 1 - 3], comprising:

a current measuring device [2 of Fig. 1; page 6, line 26 - page 7, line 1] for measuring an instantaneous current consumption of the circuit configuration [1 of Fig. 1] [page 4, line 25 - page 5, line 2];

means for comparing [12 of Fig. 1] the instantaneous current measured by said current measuring device [2 of Fig. 1] with a definable threshold value [page 8, lines 7 - 10];

a controllable clock supply circuit [4 of Figs. 1 and 2] having:

> an output [6 of Figs. 1 and 2] to be connected to a clock input [11 of Fig. 1] of the circuit configuration [1 of Fig. 1] [page 7, lines 5 - 7];
>
> a clock generator [7 of Fig. 2] generating a clock signal with clock pulses, said clock generator [7 of Fig. 2] generating a constant maximum internal frequency [See Fig. 2] [page 7, lines 24 - 26]; and
>
> a pulse filter [8 of Fig. 2] connected between said clock generator [7 of Fig. 2] and said output [6 of Figs. 1 and 2], said pulse filter [8 of Fig. 2] including a control input [5 of Figs. 1 and 2] [page 7, line 26 - page 8, line 5];

a control device [3 of Fig. 1] connected to said clock supply circuit [4 of Figs. 1 and 2] and driving said clock supply circuit [4 of Figs. 1 and 2] based upon the measured current consumption [page 7, lines 1 - 15], said control device [3 of Fig. 1] programmed to provide a control signal to said control input [5 of Figs. 1 and 2] of said pulse filter [8 of Fig. 2] when said means for comparing [12 of Fig. 1] determine that the instantaneous current consumption exceeds the definable threshold value [from 13 of Fig. 1] [page 7, lines 9 - 15]; and

said pulse filter [8 of Fig. 2] filtering out individual clock pulses [page 7, line 26 - page 8, line 5] of said clock signal generated by said clock signal generator [7 of Fig. 2], in response to said control signal at said control input [5 of Figs. 1 and 2], such that, said control device [3 of Fig. 1] adjusts said clock frequency to provide at said output [6 of Figs. 1 and 2], at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit [1 of Fig. 1] [page 5, lines 2 - 5; page 7, lines 9 - 21].

Page 6 of the instant application, in the paragraph starting at line 21, discloses that in FIG. 1, there is shown a frequency regulating circuit according to the invention. The circuit configuration 1 has a voltage supply input 10 and a clock input 11. The voltage supply input 10 is connected to an operating voltage U_B. A current I taken up by the circuit configuration 1 is measured by a current measuring device 2. A control device 3 converts the measurement result of the current measuring device 2 into a control signal for a clock supply circuit 4. To that end, the control device is connected to a control input 5 of the clock supply circuit 4. A clock output 6 of the clock supply circuit 4 is, in turn, connected to the clock input 11 of the circuit configuration 1.

Page 7 of the instant application, in the paragraph starting at line 9, discloses that When computational operations that have a high current demand are carried out in the circuit configuration 1, the demand is detected by the current measuring device 2 and, provided that this results in exceeding the maximum permissible current, the control device 3 drives the clock supply circuit 4 such that the clock frequency made available to the circuit configuration 1 is reduced. By virtue of the reduction in

the clock frequency with which the circuit configuration 1 operates, the current consumption thereof also decreases, which decrease the measuring device 2 detects. On account of this, the clock frequency provided by the clock circuit 4 is increased again so that, at any time, a maximum possible clock frequency is made available.

Page 7 of the instant application, in the paragraph starting at line 23, discloses that a more detailed illustration of the clock supply circuit is illustrated in FIG. 2. Accordingly, the clock supply circuit has a clock generator 7, which generates a constant maximum internal frequency. Moreover, it has a pulse filter 8, which is connected to the control input 5 and the clock output 6. To reduce the clock frequency, as described with reference to FIG. 1, individual pulses of the clock signal generated by the clock generator 7 are suppressed, which leads overall to a reduction in the clock frequency.

Page 8 of the instant application, in the paragraph starting at line 7, discloses that A comparator 12 can be connected to the output of the current measuring device 2 to compare the current measured by the current measuring device 2 with a definable threshold value 13.

<u>Grounds of Rejection to be Reviewed on Appeal</u>

1. Whether or not claims 1, 3, 4, 6, 7 and 9 are obvious over U. S. Patent No. 5,761,517 to Durham et al., in view of U. S. Patent No. 5,943,203 to Wang under 35 U.S.C. § 103.

Argument:

I. Whether or not claims 1, 3, 4, 6, 7 and 9 are obvious over U. S. Patent No. 5,761,517 to Durham et al., in view of U. S. Patent No. 5,943,203 to Wang under 35 U.S.C. § 103.

A. The DURHAM and WANG references fail to teach or suggest, among other limitations of Appellants' claims, suppressing an individual clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input, as required by Appellants' independent claims 1, 4 and 7.

In item 3 of the final Office Action mailed May 11, 2007 (the "**final Office Action**"), claims 1, 3, 4, 6, 7 and 9 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 5,761,517 to Durham et al ("**DURHAM**") in view of U. S. Patent No. 5,943,203 TO Wang ("**WANG**").

Appellants respectfully traverse the above rejections.

More particularly, Applicants' claim 1 recites, among other limitations:

> a control device connected to said clock supply circuit and driving said clock supply circuit based upon the measured current consumption, **said control device providing a control signal to said control input of said pulse filter when said means for comparing determine that the instantaneous current consumption exceeds the definable threshold value**; and
>
> **said pulse filter suppressing an individual clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input**, such that said control device adjusts said clock frequency to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit. [emphasis added by Applicants]

Appellants' independent claims 4 and 7 recite similar limitations to those listed above from claim 1. As such, in all of Appellants' independent claims, **the pulse filter is <u>directly controlled</u> by the control signal** (i.e., **an <u>individual</u> pulse is filtered out <u>whenever</u> the control signal is provided** to the pulse filter, and **<u>not</u> filtered out** when the control signal is **<u>not provided</u>** to the pulse filter). The above limitations of Appellants' independent claims are neither taught, nor suggested, by the **DURHAM** and/or **WANG** references.

More particularly, pages 2 - 4 of the **final Office Action** alleged that **DURHAM** disclosed the above limitations of Appellants' claims. Appellants respectfully disagree.

In item 1 of page 2 of the **final Office Action**, it is alleged that:

> Durham also teaches the pulse filter suppressing **<u>individual</u> clock pulses** (via 7) of the clock generator (27) **in response to the control signal** at the control input (from the control device). [emphasis added by Applicants]

Further, page 3 of the **final Office Action** stated, in part, that Durham:

> . . .also teaches the pulse filter (1-7, 10-13, 20) **suppressing <u>individual</u> clock pulses** of the clock generator (27), **when a high power condition is detected** (via sensor, 18), in response to the control signal at the pulse filter's control input (new_data of registers 10-13). [emphasis added by Applicants]

However, Appellants' independent claims clearly require, among other limitations, **that the filter suppress an <u>individual</u> pulse, <u>directly in response t</u>o the receipt of a control signal**. See, for example, claim 1 of the instant application ("said pulse filter **suppressing <u>an individual</u> clock pulse** of said clock signal generated

by said clock signal generator, **__in response to__ said control signal at said control input**").

Contrary to Appellants' claimed pulse filter (which **suppresses __an__ __individual pulse__**, **__in response to__ each control signal**), col. 6 of **DURHAM,** lines 29 - 52, state:

> In the case where sensor 18 has determined that a high power condition exists, **the power$_{13}$ high signal** [A] **is provided to synchronization latches 14 and 15. Then, control state machine 16 receives a control signal** [B] **from latches 14 and 15 indicating the existence of the high power condition. Select signals** [C] **are then issued by state machine 16 to pattern generator 17 so that a bit pattern** [D] **corresponding to state level 3 can be provided by pattern generator 17. At this time, a 0111 bit pattern** [D] **output from pattern generator 17 and a 0010** [E] **is issued to the 4 bit shift register.** That is, a zero is input as the new_data in registers 10, 11 and 13. A logical one is input to register 12. The logical zero input to register 10 will cause a logical 1 to be output on the data_out port of register 10 and input to the old_data port of register 11. A logical 0 is then output to register 12 and a logical one is input to register 13 such that the logical zero is output from register 13 to AND gate 7. **It can be seen that the logical zero** [F] **will occur 25% of the time,** since 1 of the 4 bit characters causes a logical zero to be present at AND gate 7. Thus, for every fourth cycle, the active portion of the oscillator clock is negated and the system clock output on node 20 will run at an effective clock frequency of 75% of the oscillator clock. This is at state level 3. [emphasis and identifiers [A] - [F] added by Applicants]

As such, it can be seen from the foregoing quoted portion of **DURHAM**, that, in **DURHAM**, **__a multitude of control signals__** (marked as [A] - [F], by Appellants) are used to determine whether or not pulses will be suppressed by one of the shift registers. This is in contrast to Appellants' claimed invention reciting **one** control signal suppressing an individual pulse. In **DURHAM**, only the **power$_{13}$ high signal** [A] and the **control signal** [B] are indicative of a high power condition**.** However, neither the **power$_{13}$ high signal** [A] of **DURHAM,** nor the **control signal** [B] of **DURHAM**, **determines whether an individual pulse of the clock signal is**

filtered by any of the shift registers of **DURHAM**. Rather, in **DURHAM**, the determination to filter pulses is made on the basis of the **logical zero signal** [F], which depends on **a number of inputs**, in particular the 0111 bit pattern [D] output from pattern generator 17 of **DURHAM** and a 0010 [E] is issued to the 4 bit shift register of **DURHAM**.

More particularly, there are situations in the system of **DURHAM, where a high power condition is indicated, yet the current pulse is not filtered**. Inversely, in **DURHAM, a pulse might be filtered, even if a high power condition has not been indicated by a control signal**.

In summary, in **DURHAM, the pulse filter OF DURHAM is not directly controlled** (i.e, "said pulse filter suppressing **an individual clock pulse of said clock signal** generated by said clock signal generator, **in response to said control signal**") by a control signal generated in response to a high power determination (i.e., the $power_{13}$ high signal [A] of **DURHAM)**, as required by Appellants' claims.

Further, the **WANG** reference (cited in **the final Office Action** as allegedly disclosing an instantaneous current sensor) does not cure the above-discussed deficiencies of the **DURHAM** reference. More particularly, like **DURHAM, WANG** fails to teach or suggest, among other limitations of Appellants' claims, a pulse filter with a control input, **which filters an individual pulse of a clock signal, in response to a control signal indicating that an instantaneous current consumption exceeds a definable threshold value**. As such, even the

combination of **DURHAM** and **WANG** fails to teach or suggest all limitations of Appellants' independent claims.

B. <u>The combination of the DURHAM and WANG specifically teaches away from the invention of Appellants' independent claims 1, 4 and 7 and/or destroys the teachings of the primary reference</u>.

Further, not only does the combination of **DURHAM** and **WANG** fail to teach or suggest Appellants' claimed invention, but, the disclosures made in those references **specifically teach away** from Appellants' claimed invention.

More particularly, the disclosure in **DURHAM** would specifically lead a person of ordinary skill in this art away from Appellants' claimed invention. For example, col. 2 of **DURHAM**, lines 1 - 5, state:

> However, **if a power high condition occurs**, **the pattern generator alters its bit pattern output to the registers in order to <u>incrementally</u> reduce the frequency of the system clock signal**, being input to the clocked elements of the circuit. [emphasis added by Appellants]

As such, **DURHAM** discloses the use of a pattern generator and a loadable shift register, in order to incrementally throttle the clock frequency provided to an electronic circuit by means of a bit pattern output to the registers of the loadable shift register. In **DURHAM**, the bit pattern is generated by a state machine, which samples a power high signal. See, for example, col. 2 of **DURHAM,** lines 11 - 15.

As can best be seen in Figs. 2 and 4 of **DURHAM** the state machine of **DURHAM** and the loadable shift register of **DURHAM**, together, change the frequency provided to the electronic circuit **<u>in a sequence of steps</u>** (i.e., **<u>incrementally</u>**, as

disclosed in col. 2 of **DURHAM**, lines 1 - 5), and **not instantaneously**. There is no way to combine the teachings of **DURHAM**, which teaches a **stateful or stepped**, and thus, a **persistent** system, with the teachings of **WANG** (i.e., in the manner suggested in **the final Office Action**) so as to provide an **instantaneous** system, **without destroying the teachings of DURHAM**. Despite it being impermissible to combine two references, wherein the combination would destroy the teachings of those reference, such teachings also direct a person of ordinary skill in this art **away** from Appellants' claimed invention. In view of the teachings of **DURHAM** (i.e., a non-instantaneous adjustment), a person of ordinary skill in the art would not consider the use of an instantaneous current sensor to be of any benefit in the system of **DURHAM**.

As such, Appellants' claimed invention is believed to **not** be rendered obvious by the combination of **DURHAM** and **WANG.**

C. The combination of the DURHAM and WANG, in the manner made in the Office Action, would not teach, suggest or motivate a person of ordinary skill in this art to produce the invention of Appellants' independent claims 1, 4 and 7.

Further still, even if a person of ordinary skill in this art would, somehow, arguendo, replace sensor 18 of **DURHAM** with the instantaneous current sensor of **WANG** (as suggested in **the final Office Action**), that person would **not** obtain Appellants' claimed invention. Rather, the combination of **DURHAM** and **WANG,** suggested in the **final Office Action**, would result in a clock control system that would still be **stateful or stepped** (i.e., not an **instantaneous** system). In particular, under a combination of the teachings of **DURHAM** and **WANG,** a person of ordinary skill in

the art would understand that, even if the input control signal A of **DURHAM** indicated a high power condition instantaneously, the output control signal F of **DURHAM** would not. Thus, the combination of **DURHAM** and **WANG** would not teach or suggest Appellants' claimed invention.

D. A person of ordinary skill in this art would not combine the DURHAM and WANG, and thus, not produce the invention of Appellants' claims 1, 4 and 7, in the manner alleged in the final Office Action.

Further, a person of ordinary skill in this art would **not** combine **DURHAM** with **WANG**. Appellants believe that the **WANG** reference is not pertinent to the particular problem with which the skilled person was concerned at the time Appellants' invention was made.

More particularly, one main problem at hand at the time the present invention was made, was to **provide a simple, yet effective, control mechanism for a frequency regulating circuit**. The **WANG** addresses **how to measure an instantaneous current consumption**. However, a person of ordinary skill in this art would not have known that, **by measuring an instantaneous current consumption**, a frequency **regulating** circuit, as provided, for example, in **DURHAM**, could be improved in order to provide an easier, more flexible frequency regulating circuit according to Applicants' presently claimed invention.

II. Conclusion.

In view of the foregoing, it can be seen that Appellants' invention is patentable over

the **DURHAM** and **WANG** references, whether taken alone, or in any permissible combination.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of Appellants' claims 1, 4 and 7. Claims 1, 4 and 7 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1, 4 or 7.

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

If an extension of time is required for this submission, petition for extension is herewith made. Any fees due should be charged to Deposit Account No. 12-1099 of Lerner Greenberg Stemer LLP.

Respectfully submitted,

/Kerry P. Sisselman/
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Date: October 15, 2007

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Claims Appendix:

1. A frequency regulating circuit for the current-consumption-dependent clock supply of a circuit configuration, comprising:

a current measuring device for measuring an instantaneous current consumption of the circuit configuration;

means for comparing the instantaneous current measured by said current measuring device with a definable threshold value;

a controllable clock supply circuit having:

> an output to be connected to a clock input of the circuit configuration;
>
> a clock generator generating a clock signal with clock pulses, said clock generator generating a constant maximum internal frequency; and
>
> a pulse filter for filtering clock pulses from said clock signal from said clock generator, said pulse filter including a control input, a filtered clock signal being provided to said output;

a control device connected to said clock supply circuit and driving said clock supply circuit based upon the measured current consumption, said control device providing a control signal to said control input of said pulse filter when said means for

comparing determine that the instantaneous current consumption exceeds the definable threshold value; and

said pulse filter suppressing an individual clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input, such that_said control device adjusts said clock frequency to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit.

3. The frequency regulating circuit according to claim 1, wherein said means for comparing further comprise a comparator comparing the current measured by the current measuring device with the definable threshold value.

4. A frequency regulating circuit for the current-consumption-dependent clock supply of a circuit configuration, comprising:

a current measuring device for measuring an instantaneous current consumption of the circuit configuration;

means for comparing the instantaneous current measured by said current measuring device with a definable threshold value;

a controllable clock supply circuit having:

an output to be connected to a clock input of the circuit configuration;

a clock generator generating a clock signal with clock pulses, said clock generator generating a constant maximum internal frequency; and

a pulse filter connected to at least one of said clock generator and said output, for filtering clock pulses from said clock signal from said clock generator, said pulse filter including a control input, a filtered clock signal being provided to said output;

a control device connected to said clock supply circuit and driving said clock supply circuit based upon the measured current consumption, said control device programmed to provide a control signal to said control input of said pulse filter when said means for comparing determines that the instantaneous current consumption exceeds the definable threshold value; and

said pulse filter suppressing an individual clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input, such that, said control device adjusts said clock frequency to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit.

6. The frequency regulating circuit according to claim 4, wherein said means for comparing comprise a comparator comparing the current measured by the current measuring device with a definable threshold value.

7. A frequency regulating circuit for the current-consumption-dependent clock supply of a circuit configuration, comprising:

a current measuring device for measuring an instantaneous current consumption of the circuit configuration;

means for comparing the instantaneous current measured by said current measuring device with a definable threshold value;

a controllable clock supply circuit having:

> an output to be connected to a clock input of the circuit configuration;
>
> a clock generator generating a clock signal with clock pulses, said clock generator generating a constant maximum internal frequency; and
>
> a pulse filter connected between said clock generator and said output, said pulse filter including a control input;

a control device connected to said clock supply circuit and driving said clock supply circuit based upon the measured current consumption, said control device programmed to provide a control signal to said control input of said pulse filter when said means for comparing determine that the instantaneous current consumption exceeds the definable threshold value; and

said pulse filter filtering out individual clock pulses of said clock signal generated by said clock signal generator, in response to said control signal at said control input, such that, said control device adjusts said clock frequency to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit.

9. The frequency regulating circuit according to claim 7, wherein said means for comparing comprise a comparator comparing the current measured by the current measuring device with a definable threshold value.

Evidence Appendix:

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or any other evidence has been entered by the Examiner and relied upon by appellant in the appeal.

Related Proceedings Appendix:

No prior or pending appeals, interferences or judicial proceedings are in existence which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal. Accordingly, no copies of decisions rendered by a court or the Board are available.